

## Model 4298

### INPUTS

**General:** Lemo front-panel connectors. Require NIM-level inputs. Impedance,  $50 \Omega \pm 5\%$ . Direct coupled. Reflections  $< 10\%$  for risetime  $> 2$  nsec.

**CLEAR:** Resets 4298 and all 4291s in crate. Minimum width 20 nsec.

**INHIBIT:** Inhibits all Wire inputs when activated.

**EXPERIMENT COMMON:** Used as the COMMON START or COMMON STOP input. Derived from the experiment trigger. Starts system digitization. Inhibited by INH and/or system BUSY signal. COMMON START Mode: the 4291 Time Digitizers cannot be stopped during the first 200 nsec following the EXP COM input. COMMON STOP Mode: The START to the 4291s must precede the EXP COM input by at least 200 nsec.

**EXTERNAL COMMON:** Used as COMMON START or COMMON STOP input when simulated wire pulses are routed to the chamber electronics to include them in test or for AUTOTRIM. Starts system digitization. Disabled by Internal Test Mode. COMMON START Mode: EXT COM input is connected to START 1 output. STOP 1 output signal must be routed to the chamber test pulse system which then generates stop pulses to the time digitizers. COMMON STOP Mode: EXT COM input is connected to STOP 1 output. START 1 output signal must be routed to the chamber test pulse system which then generates start pulses to time digitizers.

**INTERNAL COMMON:** Used as COMMON START or COMMON STOP input when simulated wire pulses are routed internally via the test line on the CAMAC Dataway to test or AUTOTRIM. Starts system digitization. Disabled by External Test mode. COMMON START Mode: INT COM input is connected to START 2 output. STOP 2 output signal must be connected to the TEST input which routes the stop signal to the time digitizers via the test line on the CAMAC Dataway. COMMON STOP Mode: INT COM input is connected to STOP 2 output. START 2 output signal must be connected to the TEST input which routes the stop signal to the time digitizers via the test line on the CAMAC Dataway.

**TEST:** Activates the test line on the CAMAC Dataway for an internal test or AUTOTRIM sequence. This input is disabled in the external mode.

### OUTPUTS

**General:** Lemo front-panel connectors. High impedance (current source) supplies NIM-levels into  $50 \Omega$ : (0 levels =  $0 \text{ mA} \pm 2 \text{ mA}$ ; 1 level =  $16 \text{ mA} \pm 2 \text{ mA}$ ). Risetime and falltime  $< 3$  nsec. Overshoot 10%.

**START 1, 2:** Internally generated when a Test or AUTOTRIM cycle is initiated.

**STOP 1, 2:** Internally generated when a Test or AUTOTRIM cycle is initiated. Delayed from START by precision time mark generator set from TIME register. Both have independent

switch-settable delays, where STOP 1 is side-panel accessible to allow for compensation of delay when using the external mode.

**BUSY:** Double-amplitude NIM pulse generated for duration of conversion and readout.

**DATABUS I/O:** Allows cascading of multiple LeCroy dedicated Controllers or Processor to one 4299 for data or control word transfer. Cable to 4299 Interface should be LeCroy DAT-DO/50-LL and to other 4298 Controllers should DAT-DI/50-LL (or use 3M 3302/50 Flat Ribbon Cable with 3M 3425-6050 Connector or LeCroy 403 211 050 Connector). The last processor on the DATABUS requires a Terminator, DAT-TR/50.

**Side-Panel Switches:** Allows user selection of operating modes and flag bits. See User Manual for detailed setup information.

### GENERAL

**Packaging:** No. 2 RF-CAMAC module conforming to ESONE Report EUR4100E and IEEE Standard 583.

**Current Requirements:** 2.4 A at +6 V; 2.4 A at -6 V.

## Model 4299

### INPUTS

**General:** Lemo front-panel connectors. Require NIM-level inputs. Impedance,  $50 \Omega \pm 5\%$ . Direct-coupled. Reflections,  $< 10\%$  for risetime  $> 2$  nsec.

**Reset (RT):** Resets registers and clears memory. Minimum width: 20 nsec.

**Clear (CL):** Clears the memory only. Minimum width: 50 nsec.

### OUTPUTS

**General:** Lemo front-panel connectors. High impedance (current source) bridge outputs supply NIM levels into  $25 \Omega$  (0 level =  $0 \text{ nA} \pm 4 \text{ mA}$ ; 1 level =  $32 \text{ mA} \pm 4 \text{ mA}$ ). Risetime and falltimes:  $< 5$  nsec. Overshoot: 10%.

**Memory Busy (MB):** Memory Busy Signal indicates that the memory contains data or is being accessed. Front-panel MB LED also indicates status.

**Databus Busy (DB):** DATABUS Busy Signal indicates that the DATABUS BUSY is activated. Front-panel DB LED also indicates status.

**DATABUS I/O:** Allows cascading of up to 16 LeCroy dedicated controllers or processors to one 4299 for data or control word transfer. Cable to first processor or controller should be DAT-DO/50-LL (or use 3M 3302/50 Flat Ribbon Cable with 3M 3425-6050 Connector or LeCroy 403 211 050 Connector). Maximum total cable lengths should not exceed 100 m. Transfer rate is two megawords per second for total cable length of 5 m or less, slower for longer runs. (See previous pages for additional information.)